

FIG. 1  
PRIOR ART PROCESSOR BOARD CONNECTED  
TO TYPICAL SYSTEM ELEMENTS

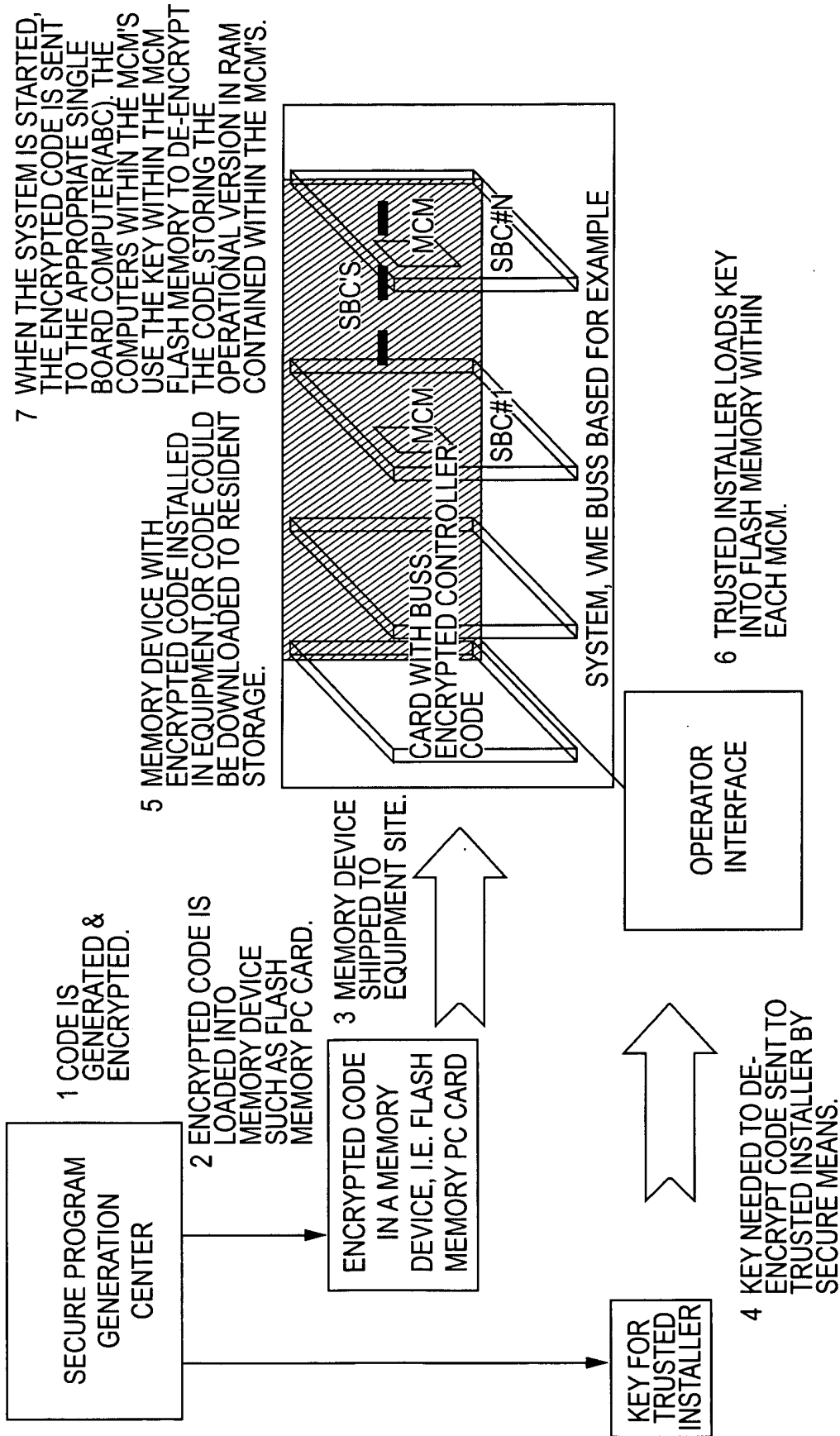


FIG. 2  
ARCHITECTURE FOR A TAMPERPROOF COMPUTER SYSTEM

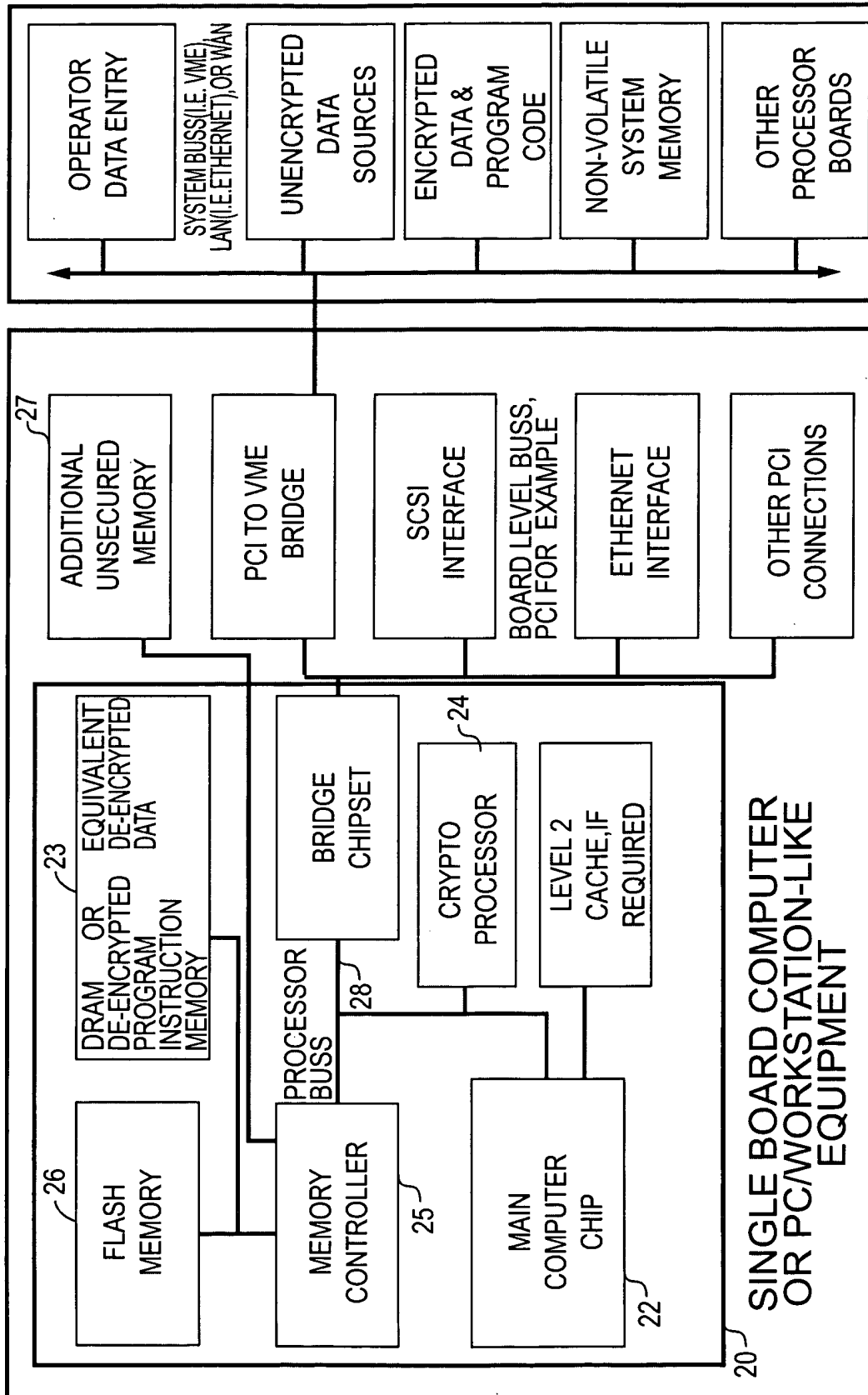


FIG. 3  
PROCESSOR BOARD WITH DE-ENCRYPTION WITHIN A  
MULTI-CHIP MODULE

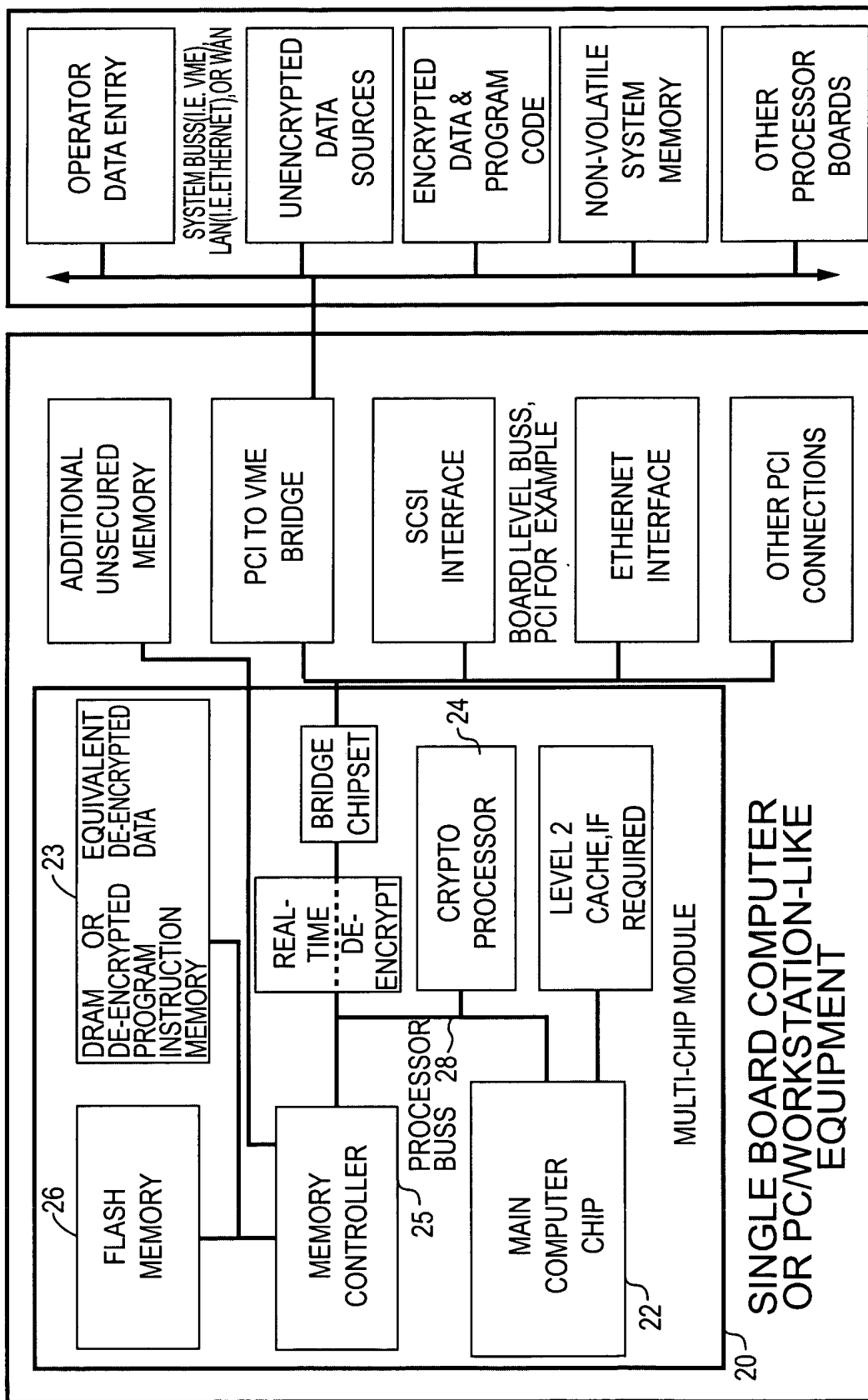
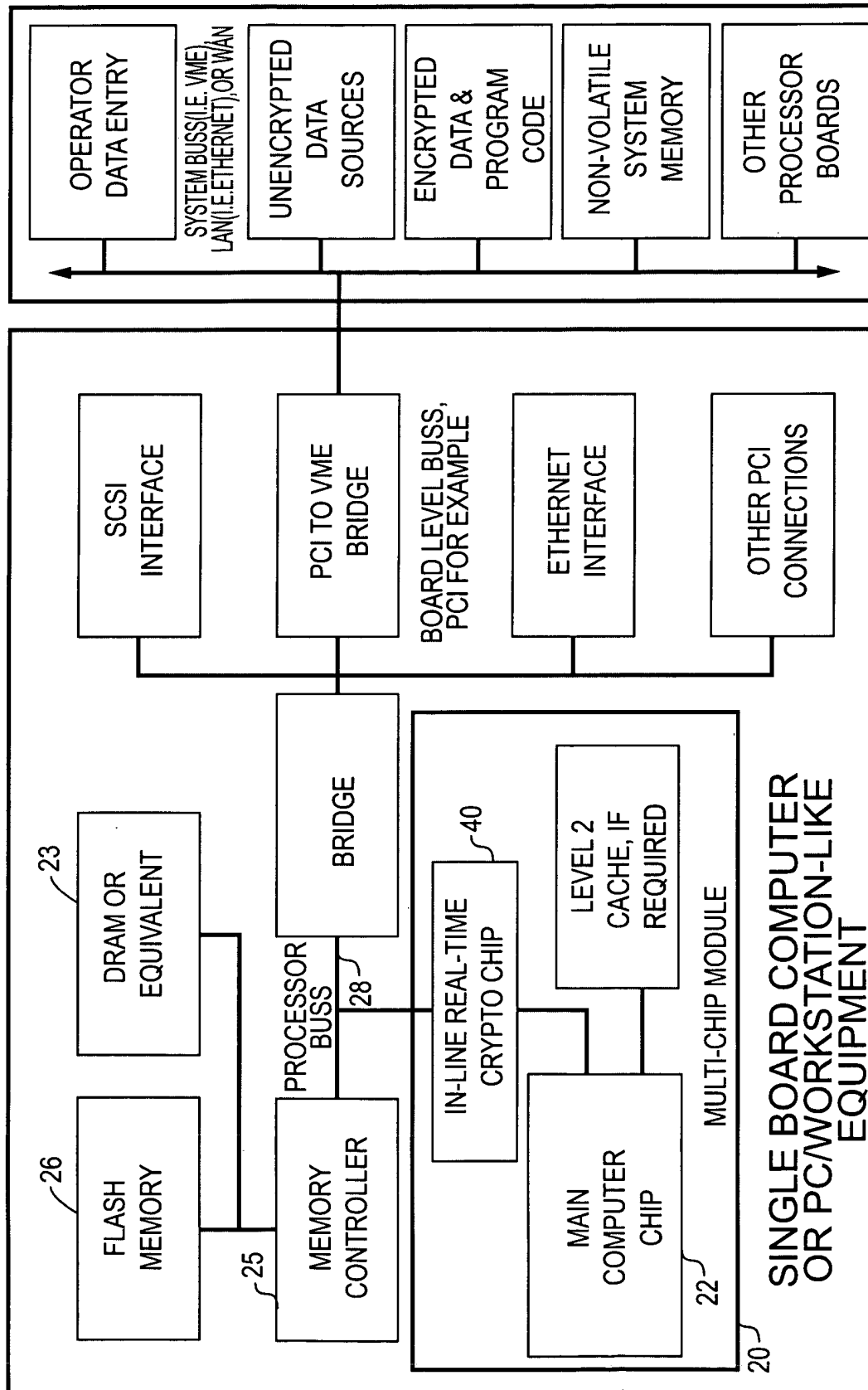


FIG. 4  
PROCESSOR BOARD WITH MULTIPLE DE-ENCRYPTION  
DEVICES WITHIN A MULTI-CHIP MODULE



**FIG. 5**  
**PROCESSOR BOARD WITH IN-LINE REAL-TIME DE-ENCRYPTION**  
**WITHIN A MULTI-CHIP MODULE**